

(1)	01/09/19	Introduction	1	BB		
(2)	02/09/19	Number System Conversion from Decimal to Other base, Other base to decimal procedures	1	BB		
(3)	03/09/19	Conversion from any base to any base sample problems	1	BB		
(4)	04/09/19	Problem Solving	1	BB		
(5)	05/09/19	Problem Solving	1	BB		
(6)	06/09/19	Complement of a number	1	BB		
(7)	07/09/19	Examples of problem solving using complements	1	BB		
(8)	08/09/19	2's & 1's complement problem solving	1	BB		
(9)	09/09/19	Problem Solving	1	BB		
(10)	10/09/19	Problem Solving	1	BB		
(11)	11/09/19	Codes BCD, BCD addition procedure problem solving	1	BB		
(12)	12/09/19	ASCII, BCD code, XS-3 code XS-3 addition problem solving	1	BB		
(13)	13/09/19	Parity code, Hamming code, error correction code				

# LESSON PLAN

Period	Date	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
(14)	23/11/14	Introduction to Logic gates	1	BB		
(15)	23/11/14	Boolean Expression construction for	2	BB		
(16)	24/11/14	Boolean theorems, Minimization of Switching function	2	BB		
(17)	24/11/14	Minimization problems.	2	BB		
(18)	24/11/14	Minimization problems	2	BB		
(19)	24/11/14	obtaining dual complement	2	BB		
(20)	24/11/14	problems on complement NAND-NOR implementation	2	BB		
(21)	24/11/14	cellular NAND-NOR realization	2	BB		
(22)	25/11/14	problem on NAND-NOR realization	2	BB		
(23)	25/11/14	SOP & POS concepts conversion.	2	BB		
(24)	25/11/14	concept of truth tables and writing equivalent form truth tables of circuit	2	BB		
(25)	26/11/14	2nd part of K-map 2 & 3 map	2	BB		
(26)	26/11/14	3, 4 - variable map problem solving	2	BB		
(27)	26/11/14	5 - variable map problem solving	2	BB		
(28)	26/11/14	problem solving	2	BB		
(29)	26/11/14	Tabular Method	2	BB		

	Topic	Chapter	No	Marking	Grade	Upon Review
(31)	11/11/14	Combinational Logic K-map	2	82		
(32)	12/11/14	Combinational design, priority	3	83		
(33)	13/11/14	Design of half, full adder, half & full parallel adder	5	85		
(34)	15/11/14	Parity bit, decoder output	6	85		
(35)	18/11/14	Carry look ahead adder	6	83		
(36)	19/11/14	BCD adder, XS-3 adder, operation	3	83		
(37)	20/11/14	design of decoder examples	6	84		
(38)	23/11/14	4 to 16 decoder using decoders	6	89		
(39)	24/11/14	16 to 64 decoder to 16 to 64 decoder	7	83		
(40)	25/11/14	Not & real time Hazard free	6	83		
(41)	30/11/14	for reduction using map	6	83		
(42)	01/12/14	problem on decoder design	6	82		
(43)	04/12/14	4 bit parity encoders	6	83		
(44)	05/12/14	decoder, for year table, example	6	85		
(45)	08/12/14	comparator	6	89		
(46)	09/12/14	Seven segment display	7	83		
(47)	15/12/14	Introduction to Sequential Logic	4	83		
(48)	16/12/14	RS latch, analysis truth table, characteristic equation	4	83		

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Period	Date (tentative)	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
(49)	6/10/14	J K latch Characteristic equation	5-9	Y BG		
(50)	13/10/14	to 1/0 D-latch, T-latch, Triggered & flip-flops, RS, D, D+T, S	5-9	Y BG		
(51)	20/10/14	flip-flop conversion excitable	4-9	Y BG		
(52)	27/10/14	Design of ripple counter	4-9	Y BG		
(53)	3/11/14	Synchronous counter r counter, 0's	4-9	Y BG		
		Shift reg. design control & buffer Reg. universal shift reg.				
(54)	10/11/14	problem solving	4-9	Y BG		
(55)	17/11/14	problems on counter and shift reg.	4-9	Y BG		
		Serial adder		Y BG		
(56)	24/11/14	Design of counter using various flip-flops	4-9	Y BG		
(57)	1/12/14	problem solving flip-flops (GATE)	4-9			
(58)	8/12/14	Introduction to VHDL programming program, multi	5	BG		
(59)	15/12/14	Design, Logic gates, writing program for	5	BG		