**LESSON PLAN**

**Subject Code & Name: Swing theory and Logic Design Branch: ECE-B**

**Class / Semester: II B.Tech I Semester Academic Year: 2014-15**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** |
|  |  | **Unit-1**  **Review of Number systems** |  |  |  |
| **1.** | **03.12.2014** | Number systems Base conversion methods | **1** | **CR** |  |
| **2.** | **04.12.2014** | Number systems Base conversion methods | **1** | **CR** |  |
| **3.** | **05.12.2014** | complements of numbers | **1** | **CR** |  |
| **4.** | **07.12.2014** | r’s, r-1’s compliment subtraction | **1** | **CR** |  |
| **5.** | **08.12.2014** | r’s, r-1’s compliment subtraction | **1** | **CR** |  |
| **6.** | **10.12.2014** | Signed binary numbers | **1** | **CR** |  |
| **7.** | **12.12.2014** | BCD | **1** | **CR** |  |
| **8.** | **14.12.2014** | Excess-3, | **1** | **CR** |  |
| **9.** | **15.12.2014** | Alphanumeric code | **1** | **CR** |  |
| **10.** | **17.12.2014** | self complement codes ,2421 | **1** | **CR** |  |
|  |  | **Unit-2**  **Logic operations error detection and correction codes** |  |  |  |
| **11.** | **18.12.2014** | Basic logic operations | **2** | **CR** |  |
| **12.** | **19.12.2014** | Logic Gates | **2** | **CR** |  |
| **13.** | **21.12.2014** | Boolean theorems, Complements, dual of logic expressions | **2** | **CR** |  |
| **14.** | **23.12.2014** | NAND,NOR XOR,XNOR gates | **2** | **CR** |  |
| **15.** | **24.12.2014** | standard SOP, POS | **2** | **CR** |  |
| **16.** | **25.12.2014** | Minimization of logic functions using theorems | **2** | **CR** |  |
| **17.** | **26.12.2014** | Self dual | **2** | **CR** |  |
| **18.** | **28.12.2014** | Gray code, error detection and correction codes, parity codes | **2** | **CR** |  |
| **19.** | **29.12.2014** | Hamming codes | **2** | **CR** |  |
| **20.** | **31.12.2014** | Multi level NAND – NAND,NOR-NOR | **2** | **CR** |  |
| **21.** | **01.01.2015** | Multilevel realizations | **2** | **CR** |  |
|  |  | **Unit-3**  **Minimization of switching functions** |  |  |  |
| **22** | **02.01.2015** | Minimization of switching functions using K-Map | **3** | **CR** |  |
| **23.** | **04.01.2015** | Tabular minimization | **3** | **CR** |  |
| **24.** | **05.01.2015** | SOP,POS realization | **3** | **CR** |  |
| **25.** | **07.01.2015** | code converters | **3** | **CR** |  |
| **26.** | **08.01.2015** | binary multiplier using K-Map | **3** | **CR** |  |
|  |  | **Unit-4**  **Combinational logic circuits-1** |  |  |  |
| **27.** | **09.01.2015** | Design of Half adder, full adder | **4** | **CR** |  |
| **28.** | **11.01.2015** | half subtractor, full subtractor | **4** | **CR** |  |
| **29.** | **12.01.2015** | applications of full adders | **4** | **CR** |  |
| **30.** | **18.01.2015** | 4-bit binary adder, | **4** | **CR** |  |
| **31.** | **19.01.2015** | 4-bit binary subtractor, | **4** | **CR** |  |
| **32.** | **21.01.2015** | adder-subtractor circuit | **4** | **CR** |  |
| **33.** | **22.01.2015** | BCD adder circuit, | **4** | **CR** |  |
| **34.** | **23.01.2015** | Excess3 adder circuit,. | **4** | **CR** |  |
| **35.** | **25.01.2015** | look-a-head adder circuit | **4** | **CR** |  |
|  |  | **Unit-5**  **Combinational logic circuits-2** |  |  |  |
| **36.** | **04.02.2015** | Design of decoder | **5** | **CR** |  |
| **37.** | **05.02.2015** | Encoder | **5** |  |  |
| **38.** | **06.02.2015** | Multiplexer | **5** | **CR** |  |
| **39.** | **08.02.2015** | Multiplexer | **5** |  |  |
| **40.** | **09.02.2015** | Multiplexer | **5** | **CR** |  |
| **41.** | **11.02.2015** | De-multiplexer | **5** | **CR** |  |
| **42.** | **12.02.2015** | Priority encoder | **5** | **CR** |  |
|  |  | **Unit-6**  **Combinational logic circuits-3** |  |  |  |
| **43.** | **13.02.2015** | PROM,PLA,PAL | **6** | **CR** |  |
| **44.** | **15.02.2015** | Realization of switching functions using PROM,PLA,PAL | **6** | **CR** |  |
| **45.** | **16.02.2015** | Comparasion PROM,PLA,PAL | **6** |  |  |
| **46.** | **18.02.2015** | Programming table | **6** | **CR** |  |
|  |  | **Unit-7**  **Sequential logic circuits-1** |  |  |  |
| **47.** | **19.02.2015** | Classification of sequential circuits, Flip-flops with truth table | **7** | **CR** |  |
| **48.** | **20.02.2015** | Conversion of flip-flop to flip-flop. | **7** | **CR** |  |
| **49.** | **22.02.2015** | Design of ripple counters | **7** | **CR** |  |
| **50.** | **23.02.2015** | Synchronous counters | **7** |  |  |
| **51.** | **25.02.2015** | Synchronous counters | **7** | **CR** |  |
| **52.** | **26.02.2015** | Johnson counters | **7** | **CR** |  |
| **53.** | **27.02.2015** | ring counters | **7** | **CR** |  |
| **54.** | **01.03.2015** | Design of Buffer register, | **7** | **CR** |  |
| **55.** | **03.03.2015** | control buffer register, | **7** | **CR** |  |
| **56.** | **04.03.2015** | Shift register,. | **7** | **CR** |  |
| **57.** | **05.03.2015** | Bi-directional shift register | **7** | **CR** |  |
| **58.** | **06.03.2015** | Universal shift register | **7** | **CR** |  |
|  |  | **Unit-8**  **Sequential logic circuits-II** |  |  |  |
| **59.** | **08.03.2015** | FSM | **8** | **CR** |  |
| **60.** | **09.03.2015** | Capabilities and limitations | **8** | **CR** |  |
| **61** | **11.03.2015** | Capabilities and limitations | **8** | **CR** |  |
| **62** | **12.03.2015** | State tables | **8** | **CR** |  |
| **63** | **13.03.2015** | State tables | **8** | **CR** |  |
| **64** | **15.03.2015** | Realization using FFs | **8** | **CR** |  |
| **65** | **16.03.2015** | Realization using FFs | **8** | **CR** |  |
| **66** | **18.03.2015** | Melay to moore conversion | **8** | **CR** |  |
| **67** | **19.03.2015** | Moore to Melay conversion | **8** | **CR** |  |