

LESSON PLAN

Branch: I M.Tech

Semester: II

Subject : AVDA

Academic year: 2014-15

faculty :Swathi jallu

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action upon Review
		PRELIMINARIES	I			
1.	30.03.2015	Introduction to Design Methodologies The VLSI Design problem Gaskis Y-Chart	I	Black Board		
2.	31.03.2015	The VLSI Design problem Gaskis Y-Chart	I	B.B		
3.	01.04.2015	Design Actions ,Design methods and Technologies.	I	B.B		
4.	06.04.2015	VLSI Design Automation tools	I	B.B		
5.	07.04.2015	Tr-level design layout design, verification.	I	B.B		
6.	08.04.2015	Algorithm Graph Theroy and Terminology	I	B.B		
7.	10.04.2015	Dta Structures for the representation of graphs, Computational Complexity	I	B.B		
8.	13.04.2015	Graph algorithms-DFS,BFS				
9.	15.04.2015	Dijkstra's shortest path algorithm, prims algorithm	I	B.B		
10.	17.04.2015	Tractable and Intractable Problems	I	B.B		
		GENERAL PURPOSE METHOD FOR COMBINATIONAL OPTIMIZATION	II			
11.	20.04.2015	Introduction		B.B		
12.	21.04.2015	Travelling salesman problem Backtracking	II	B.B		
13.	22.04.2015	Branch and Bound,	II	B.B		
14.	24.04.2015	Dynamic Programming	II	B.B		
15.	27.04.2015	Integer Linear Programming	II	B.B		
16.	28.04.2015	Local Search	II	B.B		
17.	29.04.2015	Simulated Annealing	II	B.B		
18.	01.05.2015	Tabu search, Genetic Algorithms	II	B.B		

		Layout compaction, symbol layout	III			
19.	18.05.2015	Introduction	III	B.B		
20.	19.05.2015	Bellman-fold algorithm liao-wong algorithm	III	B.B		
21.	20.05.2015	Placement and partitioning	III	B.B		
22.	22.05.2015	Placement algorithm & partitioning the Kernighan-lin partitioning Algorithm	III	B.B		
23.	25.05.2015	Floorplanning concepts	III	B.B		
24.	26.05.2015	Routing, area routing algorithms	III	B.B		
25.	27.05.2015	Global routing algorithms	III	B.B		
26.	29.05.2015	Modelling and simulation, Gate Level Modeling	III	B.B		
27.	08.06.2015	Simulation, compiler driven and event driven simulation	III	B.B		
28.	09.06.2015	Switch level Modeling and simulation.	III	B.B		
		LOGIC SYNTHESIS AND VERIFICATION	IV			
29.	10.06.2015	Introduction	IV	B.B		
30.	12.06.2015	Basic issues and Terminology,	IV	B.B		
31.	15.06.2015	Binary-Decision diagram	IV	B.B		
32.	16.06.2015	ROBDD principles, construction, and variable ordering and Transition count testing,	IV	B.B		
33.	17.06.2015	Two – Level Logic Synthesis.	IV	B.B		
34.	19.06.2015	High Level Logic Synthesis.	IV	B.B		
35.	22.06.2015	Internal representation of the input algorithm	IV	B.B		
36.	23.06.2015	Allocation ,assignment and scheduling	IV	B.B		
37.	24.06.2015	Some Scheduling algorithms and High level Trannsformations.	IV	B.B		
		PHYSICAL DESIGN AUTOMATION OF FPGA'S	V			
38.	26.06.2015	FPGA Introduction	V	B.B		
39.	29.06.2015	FPGA technologies,	V	B.B		
40.	30.06.2015	Physical Design cycle for FPGA's	V	B.B		
41.	01.07.2015	partitioning and routing for	V	B.B		

		segmented models				
42.	03.07.2015	Routing algorithm	V	B.B		
43.	06.07.2015	partitioning and routing for staggered models.	V	B.B		
44.	07.07.2015	algorithm for segmented models and staggered models.	V	B.B		
		PHYSICAL DESIGN AUTOMATION OF MCM'S:	VI			
45	08.07.2015	MCM technologies	VI			
46	13.07.2015	MCM physical design cycle and partitioning.	VI	B.B		
47	14.07.2015	Placement – Chip array based full custom approaches,	VI	B.B		
48	15.07.2015	Routing – Maze routing, Multiple stage routing	VI	B.B		
49	17.07.2015	Topologic routing, Integrated Pin – Distribution and Routing.	VI	B.B		
50	20.07.2015	Routing of FMCM's programmable MCM's	VI	B.B		

CR: CLASS ROOM

PPT: POWER POINT PRESENTATION

LCD

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, Johnwiley& Sons (Asia) Pvt. Ltd, 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer International Edition, 2005

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

FACULTY

HEAD OF THE DEPARTMENT