

# LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	26/08	CMOS logic	I	B-B		
		Introduction to logic families				
2	27/08	CMOS logic		B-B		
3	27/08	CMOS steady state electrical behaviour		B-B		
4	28/08	- do -		B-B		
5	29/08	CMOS logic gates NOT		B-B		
6	01/09	CMOS dynamic electrical behaviour		B-B		
7	02/09	CMOS logic families		B-B		
8	03/09	CMOS logic gates NAND, NOR		B-B		
9	04/09	AND, OR		B-B		
10	05/09	problems		B-B		
11	08/09	Bipolar logic Diode logic	II	B-B		
12	09/09	Bipolar logic		B-B		
13	09/09	Transistor logic		B-B		
14	10/09	TTL families		B-B		
15	11/09	CMOS / TTL interfacing		B-B		
16	12/09	Low voltage CMOS logic and interfacing		B-B		

facin g

# LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
17	15/09	Emitter coupled logic		B-B		
18	16/09	Comparison of logic families		B-B		
19	17/09	Familiarity with standard 74xx, 40xx		B-B		
20	18/09	TTL NAND, NOR		B-B		
21	19/09	COMBINATIONAL logic Design I Introduction	<u>III</u>	B-B		
22	21/09	Design and Analysis procedure		B-B		
23	23/09	Decoders		B-B		
24	23/09	encoders		B-B		
25	25/09	finite State Devices		B-B		
26	26/09	MUX, DeMUX		B-B		
27	29/09	Code converters EX-OR gates		B-B		
28	30/09	parity, comparison.		B-B		
29	30/09	Adders & Subtraction		B-B		
30	02/10	Design of CS logic circuits. Using IC's		B-B		
31	04/10	CS-II Ripple Adder	<u>IV</u>	B-B		
32	06/10	Look ahead carry adder		B-B		
33	07/10	Binary parallel Adder n-bit parallel subtraction		B-B		
34	07/10	ALUs, combination multipliers		B-B		
35	09/10	Barrel shifter Simple Handing point		B-B		
36	10/10	Encoders		B-B		

# LESSON PLAN

Period	Date (tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
37	11/10	cascading comp	<u>IV</u>	B-B		
38	12/10	dual priority Encoder		B-B		
39	13/10	about logic circuits using ICS		B-B		
40	14/10	sequential logic D-I Introduction	<u>V</u>	B-B		
41	15/10	The basic bistable element		B-B		
42	16/10	latches, Flip-flops		B-B		
43	18/10	SSE latches, D-F		B-B		
44	19/10	Counters		B-B		
45	21/10	Applications		B-B		
46	03/11	Synchronous design methodology		B-B		
47	04/11	Impediments to Synchronous design		B-B		
48	05/11	Design using ICS		B-B		
49	06/11	S-L-D-II MSR Register	<u>VI</u>	B-B		
50	07/11	Shift Registers		B-B		
51	08/11	modes of operation		B-B		
52	09/11	Universal Shift Register		B-B		
53	10/11	Ring counter		B-B		

# LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
53	11/11	Johnson counter	<u>VI</u>	B-B		
54	11/11	Basic sequential logic Design steps		B-B		
55	13/11	Design of modulus 2 synchronous counter		B-B		
56	14/11	Circuits using relevant ICs		B-B		
57	17/11	PLDs	<u>VII</u>			
		Introduction		B-B		
58	18/11	PROM	<u>VII</u>	B-B		
59	18/11	PLA		B-B		
60	20/11	PAL		B-B		
61	21/11	Comparison of		B-B		
		PROM, PLA, PAL		B-B		
62	24/11	PLDs with		B-B		
		relevant ICs				
63	25/11	MEMORIES ROM	<u>VIII</u>			
64	25/11	Internal structure		B-B		
65	27/11	2D - Decoding		B-B		
66	28/11	Commercial ROM types		B-B		
		Timing Applications				

## LESSON PLAN

[illegible]