**LESSON PLAN**

**Branch**: III ECE ‘C’ **Semester**: II **Subject** : VLSI

**Acadamic year:2014-15 faculty :A.JAYALAXMI**

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| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|  |  | **Introduction** | I |  |  |  |
|  | 19.01.2015 | Introduction to IC Technology The IC era, MOS and related VLSI technology | I | Black Board |  |  |
|  | 20.01.2015 | Basic MOS transistors. | I | B.B |  |  |
| 3-5 | 08.01.2015 to  22.01.2015 | IC production process | I | B.B |  |  |
| 6 | 26.01.2015 to  28.01.2015 | MOS and CMOS fabrication process. | I | B.B |  |  |
| 7 | 29.01.2015 | Bi-CMOS technology | I | B.B |  |  |
| 8 | 29.01.2015 | Comparison between CMOS and bipolar technologies. | I | B.B |  |  |
|  |  | **Basic electrical properties of MOS and Bi-CMOS circuits** | II |  |  |  |
| 9 | 30.01.2015 | Ids – Vds relationship | II | B.B |  |  |
| 10 | 02.02.2015 | Aspects of MOS transistor: threshold voltage | II | B.B |  |  |
| 11 | 03.02.2015 | trans-conductance, output conductance and figure of merit.Pass transistor, | II | B.B |  |  |
| 12 | 04.02.2015 | MOS inverter ,Determination of pull-up to pull-down ratio of NMOS. | II | B.B |  |  |
| 13 | 05.02.2015 | NMOS inverter driven by another NMOS inverter and driven through one or more pass transistors | II | B.B |  |  |
| 14 | 06.02.2015 | Alternative forms of pull-up | II | B.B |  |  |
| 15 | 09.02.2015 | CMOS inverter, MOS transistor circuit model | II | B.B |  |  |
| 16 | 10.02.2015 | Bi-CMOS inverter and latch-up in CMOS circuits, susceptibility | II | B.B |  |  |
| 17 | 11.02.2015 | **Mos & Bicmos Circuits Design Process:** MOS layers | III | B.B |  |  |
| 18 | 12.02.2015 | stick diagrams | III |  |  |  |
| 19 | 13.02.2015 | Design rules and layouts | III | B.B |  |  |
| 20 | 16.02.2015 | 2 micro meter Design rules | III |  |  |  |
| 21 | 18.02.2015 | 1.2 micro meter Design rules | III | B.B |  |  |
| 22 | 19.02.2015 | layout diagrams for NMOS | III | B.B |  |  |
| 23 | 20.02.2015 | CMOS inverters and gates. | III | B.B |  |  |
| 24 | 23.02.2015 | Symbolic diagrams translation to mask forms |  |  |  |  |
| 25 | 24.02.2015 | **Basic circuit concepts:** Sheet resistance (Rs) and its concept to MOS | IV | B.B |  |  |
| 26 | 25.02.2015 | Area capacitance calculations, | IV | B.B |  |  |
| 27 | 26.02.2015 | Standard units of capacitance calculation | IV | B.B |  |  |
| 28 | 27.02.2015 | driving large capacitive load wiringcapacitances,propogation delays,wiring capacitances | IV | B.B |  |  |
| 29 | 02.03.2015 | Fan-in and fan-out, Choice of layers ,transistor switches | IV | B.B |  |  |
| 30 | 03.03.2015 | Realization of gates using nmos,pmos,cmos | IV |  |  |  |
| 31 | 04.03.2015 | **Scaling of MOS circuits:** Scaling models & scaling factors for device parameters | V |  |  |  |
| 32 | 05.03.2015 | Limitations of Scaling | V | B.B |  |  |
| 33 | 06.03.2015 | Limits due to subthreshold current, logic levels & supply voltage due to noise ,current density | V | B.B |  |  |
| 34 | 16.03.2015 | Some Architecture issues | V | B.B |  |  |
| 35 | 17.03.2015 | Some Architecture issues | V | B.B |  |  |
| 36 | 18.03.2015 | Introduction to switch logic and gate logic | V | B.B |  |  |
| 37 | 19.03.2015 | Introduction to switch logic and gate logic | V | B.B |  |  |
| 38 | 20.03.2015 | **Semiconductor integrated circuit design:**Introduction to PLA,PAL,PLDs | VI | B.B |  |  |
| 39 | 23.03.2015 | Full custom design, Semi custom design | VI | B.B |  |  |
| 40 | 24.03.2015 | Gate arrays, standard cells | VI | B.B |  |  |
| 41 | 25.03.2015 | CPLDs,FPGAs | VI | B.B |  |  |
| 42 | 26.04.2015 | Design issues | VI | B.B |  |  |
| 43 | 27.04.2015 | Design issues | VI | B.B |  |  |
| 44 | 30.03.2015 | **Digital design using HDL:**DSD processors | VII | B.B |  |  |
| 45 | 31.03.2015 | VLSI circuits design process | VII | B.B |  |  |
| 46 | 01.04.2015 | Hard ware simulation | VII | B.B |  |  |
| 47 | 03.04.2015 | Hard ware synthesis | VII |  |  |  |
| 48 | 06.04.2015 | History of VHDL | VII | B.B |  |  |
| 49 | 07.04.2015 | HDL requirements | VII | B.B |  |  |
| 50 | 08.04.2015 | Level of abstract | VII | B.B |  |  |
| 51 | 09.04.2015 | Elements of VHDL,packages, | VII | B.B |  |  |
| 52 | 10.04.2015 | libraries ans bindings,objectsand classes, | VII | B.B |  |  |
| 53 | 13.04.2015 | variable assignments,sequential statements,usage of subprograms, | VII | B.B |  |  |
| 54 | 14.04.2015 | comparision of VHDL and verilog | VII | B.B |  |  |
| 55 | 16.04.2015 | **VHDL modelling:** simulation | VII | B.B |  |  |
| 56 | 17.04.2015 | Logic synthesis inside a logic synthesisor, | VII | B.B |  |  |
| 57 | 20.04.2015 | constraints,technology libraraies, | VII | B.B |  |  |
| 58 | 21.04.2015 | VHDL and logic synthesis, | VII | B.B |  |  |
| 59 | 22.04.2015 | functional gate level verification, | VII | B.B |  |  |
| 60 | 23.04.2015 | place and route, | VII | B.B |  |  |
| 61 | 24.04.2015 | post layout timing simulation,static timing, | VII | B.B |  |  |
| 62 | 27.04.2015 | major netlist formats for design representation, | VII | B.B |  |  |
| 63 | 28.04.2015 | major netlist formats for design representation, | VII | B.B |  |  |
| 64 | 29.04.2015 | VHDL synthesis | VII | B.B |  |  |
| 65 | 30.04.2015 | program approach | VII | B.B |  |  |
| 66 | 1.05.2015 | program approach | VII | B.B |  |  |

**Text books:**

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005.
2. Principles of CMOS VLSI Design – Weste and Eshraghian, Pearson Education, 1999.

**Reference books:**

1. VLSI Design – Debaprasad Das, Oxford university press, 2010.
2. VLSI Design – A.Albert Raj and T.Latha, PHI Learing private limited 2010.
3. ASIC design - Smith.