**LESSON PLAN**

**Subject Code & Name: CPLD & FPGA**

**Branch: VLSI & DECS Class / Semester: I-M.Tech-SEM II Academic Year:2014-15**

**Faculty: K.KRISHNAMRAJU**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **PROGRAMMABLE LOGIC DEVICES** | **I** |  |  |  |
| 1 | 30-3-15 | Introduction |  | BB |  |  |
| 2 | 31-3-15 | ROM, PLA, PAL– Features |  | BB |  |  |
| 3 | 01-4-15 | CPLD, FPGA – Features |  | BB |  |  |
| 4 | 06-4-15 | Architectures |  | BB |  |  |
| 5 | 07-4-15 | Programming |  | BB |  |  |
| 6 | 07-4-15 | Applications |  | BB |  |  |
| 7 | 08-4-15 | Implementation of MSI circuits using Programmable logic Devices. |  | BB |  |  |
|  | 08-4-15 | **CPLDs** | **II** | BB |  |  |
| 8 | 9-4-15 | Complex Programmable Logic Devices, Altera series |  | BB |  |  |
| 9 | 13-4-15 | Max 5000/7000 series and Altera FLEX logic |  | BB |  |  |
| 10 | 15-4-15 | 10000 series CPLD AMD’s |  | BB |  |  |
| 11 | 17-4-15 | CPLD (Mach 1 to 5), |  | BB |  |  |
| 12 | 20-4-15 | Cypress FLASH 370 Device technology, |  | BB |  |  |
| 13 | 21-4-15 | Lattice pLSI’s architectures –3000 series |  | BB |  |  |
| 14 | 22-4-15 | Speed performance and in system programmability |  | BB |  |  |
|  | 24-4-15 | **FPGAs** | **III** | BB |  |  |
| 15 | 28-4-15 | Field Programmable Gate Arrays- |  | BB |  |  |
| 16 | 01-5-15 | Logic blocks, |  | BB |  |  |
| 17 | 18-5-15 | routing architecture, |  | BB |  |  |
| 18 | 19-5-15 | design flow |  | BB |  |  |
| 19 | 19-5-15 | technology mapping for FPGAs, |  | BB |  |  |
| 20 | 08-6-15 | Case studies Xilinx XC4000 & ALTERA’s |  | BB |  |  |
| 21 | 06-06-15 | FLEX 8000/10000, FPGAs: AT &T ORCA’s |  | BB |  |  |
|  | 06-06-15 | **FINITE STATE MACHINES (FSM)** | **IV** |  |  |  |
| 22 | 06-06-15 | Top Down Design, State Transition Table, |  | BB |  |  |
| 23 | 06-06-15 | State assignments for FPGAs, |  | BB |  |  |
| 24 | 09-06-15 | Realization of state machine charts using PAL |  | BB |  |  |
| 25 | 10-06-15 | Alternative realization for state machine charts using microprogramming, |  | BB |  |  |
| 26 | 12-6-15 | linked state machine, encoded state machine. |  | BB |  |  |
| 27 | 17-6-15 | FSM ARCHITECTURES: Architectures Centered around non registered PLDs, |  | BB |  |  |
| 28 | 19-6-15 | Design of state machines centered around shift registers |  | BB |  |  |
| 29 | 22-6-15 | One Hot state machine, |  | BB |  |  |
| 30 | 22-6-15 | Petrinets for state machines-Basic concepts and properties, |  | BB |  |  |
| 31 | 23-6-15 | Finite State Machine-Case study. |  | BB |  |  |
|  | 24-6-15 | **DESIGN METHODS** | **V** |  |  |  |
| 32 | 24-6-15 | Introduction |  | BB |  |  |
| 33 | 26-6-15 | : One –hot design method, |  | BB |  |  |
| 34 | 29-6-15 | Use of ASMs in one-hot design method, |  | BB |  |  |
| 35 | 30-6-15 | Applications of one hot design method, |  | BB |  |  |
| 36 | 3-7-15 | Extended Petri-nets for parallel controllers, |  | BB |  |  |
| 37 | 06-7-15 | Meta Stability, |  | BB |  |  |
| 38 | 7-7-15 | Synchronization, |  | BB |  |  |
| 39 | 8-7-15 | Complex design using shift registers. |  | BB |  |  |
|  | 10-7-15 | SYSTEM LEVEL DESIGN: | **VI** |  |  |  |
| 40 | 13-7-15 | Controller, data path designing, |  | BB |  |  |
| 41 | 14-7-15 | Functional partition, |  | BB |  |  |
| 42 | 15-7-15 | Digital front end digital design tools for FPGAs & ASICs, |  | BB |  |  |
| 43 | 17-7-15 | System level design using mentor graphics EDA tool(FPGA Advantage), |  | BB |  |  |
| 44 | 20-7-15 | Design flow using CPLDs and FPGAs. |  | BB |  |  |
| 45 | 21-7-15 | CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder |  | BB |  |  |
| 46 | 22-7-15 | parallel adder sequential circuits, counters |  | BB |  |  |
| 47 | 24-7-15 | parallel adder sequential circuits, Multiplexers parallel Controllers |  | BB |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**TEXT BOOKS:**

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.

3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

**REFERENCES BOOKS:**

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad,1994, Prentice Hall.

2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007,BSP.

**FACULTY HEAD OF THE DEPARTMENT**