

LESSON PLAN

BB - Black Board

PPT - Power point presentation

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	30.3.15	Overview of	I	BB		
		LP, VLSI.	"	"		
2	31.3.15	Introduction to low power, low	"	"		
		voltage design.	"	"		
3	1.4.15	low voltage, low power limitations	"	"		
4	2.4.15	Power supply, threshold voltage limitations	"	PPT		
5	3.4.15	Scaling & Interconnect Limitations	"	BB		
6	4.4.15	SoI CMOS as a replacement	"	"		
7	5.4.15	Integration & Realization	"	PPT		
8	6.4.15	Integrated CMOS process	"	BB		
9	7.4.15	Analog / Digital CMOS process	"	"		
10	8.4.15	Low voltage / power BiCMOS process	II	BB		
11	9.4.15	Realization of BiCMOS process.	"	"		
12	10.4.15	Low cost, low power medium speed BiCMOS	"	"		
13	11.4.15	High performance Digital BiCMOS process	"	PPT		
14	12.4.15	Realization of BiCMOS process.	"	BB		
15	13.4.15	SoI CMOS / BiCMOS VLSI	"	"		
16	14.4.15	Lateral ST on SoI	"	"		
17	15.4.15	Future trends & direction CMOS / BiCMOS process	"	"		
18	16.4.15	Introduction to device behaviour & modelling	III	PPT		

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19	1.5.15	over view of the mos transistor summer vacatins	III	PPT 4.5.15	to 10.5.15	
20	19.5.15	Static & Dynamic Characteristics	"	BB		
21	20.5.15	MOSFET Spice models, Level 1, 4, 5, 6.	"	"		
22	21.5.15	Advanced MOSFET models.	"	"		
23	22.5.15	UDICE, EKV model & Equations.	"	"		
24	26.5.15	Bipolar Spice models, Ebers mole, Gummel post. model	"	"		
25	27.5.15	Surface p-channel for sub-threshold micro model	"	"		
26	28.5.15	Introduction to Subthreshold Mos device	IV	BB		
27	29.5.15	Device fabrication model parameters mid Exam	"	1-6.15 to 6/6/15		
28	2-6-15 9.6.15	Sub-threshold micro dc model formulation	"	"		
29	10.6.15	Analytical Characterisation of submicron MOS device	"	PPT		
30	11.6.15	Experimental Characterisation of Mos device	"	PPT		
31	12.6.15	Modified Gummel post model.	"	BB		
32	16.6.15	MOSFET in	"	"		
33	17.6.15	Hybrid mode Environment	"	"		
34	18.6.15	Introduction to low voltage &	V	"		
35	19.6.15	Low power logic Circuits.	"	"		
36	23.6.15	Digital Circuits design by CMOS	"	"		
37	24.6.15	Full swing multi drain BiCMOS buffers	"	"		
38	25.6.15	Quasi-complementary BiCMOS digital cells	"	"		

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39	26.6.15	High-Area CMOS Digital Circuits	II	B.D		
40	30.6.15	Transiently Saturated Pushing CMOS Circuits	"	PPT		
41	1.7.15	Boost Strapped Type CMOS Digital Circuits	"	"		
42	2.7.15	ESD free CMOS Circuits	"	AB		
43	3.7.15	Comparative Evolution of Digital Circuits	"	"		
44	7.7.15	Introduction to Low Voltage Low power	VI	"		
45	8.7.15	Logic Circuits	"	"		
46	9.7.15	Evolution of Latches & Flip-Flops	"	"		
47	10.7.15	Optimization, Performance Pipeline Theme	"	"		
48	14.7.15	Conventional CMOS Logic Circuits	II	"		
49	15.7.15	Conventional CMOS Logic Gates	"	PPT		
50	16.7.15	Performance Evolution	"	AB		
51	19.7.15	of Logic Gate Circuits	"	"		
52	21.7.15	Quality measures for Latches & FFs	"	"		
53	22.7.15	Performance measures	"	"		
54	23.7.15	Power dissipation & Area measures	"	"		
55	24.7.15	Design Perspectives of Latches & FFs	"	"		
			II			