

LESSON PLAN

BD - Blackboard

PPT - power point presentation

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	22/8/16	Introduction to IC Design	I	BB		
2	23/8/16	Historical Perspective of ICs	"	"		
3	26/8/16	Design in MCMC Integrated circuit	"	"		
4	29/8/16	Logic models of MCMC Design.	"	"		
5	30/8/16	Estimation of cost in circuit design	"	"		
6	1/9/16	Feasibility & design ICs	"	PPT		
7	2/9/16	Design of ICs.	"	BB		
8	6/9/16	Performance characteristics of ICs Design	"	"		
9	8/9/16	Passer Combinational Design ICs	"	"		
10	9/9/16	Timing assumptions & design ICs.	"	"		
11	12/9/16	Introduction to MOS Transistor	II	PPT		
12	13/9/16	Differentiation of PMOS, CMOS, PMOS etc	"	"		
13	15/9/16	Static CMOS Inverter.	"	"		
14	16/9/16	Qualitative perspective of CMOS Inverter	"	BB		
15	19/9/16	Evolution of CMOS Inverter Robustness.	"	"		
16	20/9/16	Characteristics of CMOS Inverter - Static ^{preliminary}	"	"		
17	22/9/16	Switching threshold, voltage margin	"	"		
18	23/9/16	Performance of CMOS Inverter - Dynamic ^{behavior}	"	"		
19	26/9/16	Capacitance - Computing.	"	"		
20	27/9/16	Introduction to CMOS ^{logic families}	III	PPT		

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21	29/9/16	Cmos-characteristics - Cmos Inverter.	IV	B B		
22	30/9/16	Static and dynamic behaviours of CMOS	"	"		
23	3/10/16	Actual mos transistor and comparison.	"	"		
24	4/10/16	Some secondary effects of CMOS transist.	"	"		
25	6/10/16	Spice models for CMOS transistors	"	PPT		
26	7/10/16	Level 3 and Level 4 models of mos transistor	"	"		
27	10/10/16	Method of logical effort for transistor	"	B.B		
28	14/10/16	Verilog, some other spice models.	"	"		
29	24/10/16	Introduction to Logic families	IV	"		
30	25/10/16	CMOS Logical families.	"	PPT		
31	27/10/16	TTL & ECL Logic families.	"	"		
32	28/10/16	Interfacing of Logic families - Inverter	"	"		
33	31/10/16	CMOS/TTL - Interfacing	"	"		
34	1/11/16	Comparabilities of Logic families.	"	B.B		
35	3/11/16	Combinational Logic Design using VHDL	"	"		
36	4/11/16	Introduction to VHDL Language	"	"		
37	7/11/16	VHDL modeling for decoders - Encoder.	"	"		
38	8/11/16	VHDL modeling for Encoder - mux - Adders.	"	"		
39	10/11/16	Sequential In design using VHDL	V	"		
40	11/11/16	VHDL modeling for Sequential circuits	"	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
41	15/11/16	VHDL modelling for latches, flipflops	V	D.D		
42	17/11/16	VHDL modelling for Counters.	"	"		
43	18/11/16	Some Examples on VHDL modelling - FSMs.	"	PPT		
44	21/11/16	Examples on ASM Charts	"	"		
45	22/11/16	Digital Integrated System Building Blocks.	"	D.D		
46	24/11/16	VHDL modelling as muxes.	"	"		
47	25/11/16	System Building Blocks - Decoders	"	"		
48	28/11/16	Serial Shifters - Counters - adders.	"	"		
49	29/11/16	Introduction to Memory.	V	PPT		
50	1/12/16	Dom - Internal Structure - Supplement	"	"		
51	2/12/16	2D decoding Commercial type memory - application	"	"		
52	5/12/16	RAM Internal Structure	"	"		
53	6/12/16	Comparisons of memory.	"	PPT		
54	8/12/16	CPLD - Introduction - Supplement	"	"		
55	9/12/16	Xc 9500 series family CPLD	"	PPT		
56	12/12/16	CLB - Internal Structure	"	"		
57	13/12/16	IO Block Internal Structure	"	"		
58	15/12/16	FPGA - Conceptual view of FPGA	"	D.D		
59	16/12/16	Architecture Based on CLB Internal Structure	"	"		