**LESSON PLAN**

**Branch**: I M.Tech **Semester**: II **Subject** : AVDA

**Acadamic year: 2016-17 faculty :D.V.L.N.Sastry**

|  |  |  |  |  |  |  |
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| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|  |  | **PRELIMINARIES** | I |  |  |  |
|  | 22.02.2017 | Introduction to Design Methodologies The VLSI Design problem Gaskis Y-Chart | I | Black Board |  |  |
|  | 23.02.2017 | The VLSI Design problem Gaskis Y-Chart | I | B.B |  |  |
|  | 24.02.2017 | Design Actions ,Design methods and Technologies. | I | B.B |  |  |
|  | 25.02.2017 | VLSI Design Automation tools | I | B.B |  |  |
|  | 25.02.2017 | Tr-level design layout design, verification. | I | B.B |  |  |
|  | 01.03.2017 | Algorithm Graph Theroy and Terminology | I | B.B |  |  |
|  | 03.03.2017 | Dta Structures for the representation of graphs, Computational Complexity | I | B.B |  |  |
|  | 04.03.2017 | Graph algorithms-DFS,BFS |  |  |  |  |
|  | 08.03.2017 | Dijkstra’s shortest path algorithm, prims algorithm | I | B.B |  |  |
|  | 10.03.2017 | Tractable and Intractable Problems | I | B.B |  |  |
|  |  | **GENERAL PURPOSE METHODS FORCOMBINATIONAL OPTIMIZATION** | II |  |  |  |
|  | 11.03.2017 | Introduction |  | B.B |  |  |
|  | 15.03.2017 | Travelling salesman problem Backtracking | II | B.B |  |  |
|  | 18.03.2017 | Branch and Bound, | II | B.B |  |  |
|  | 18.03.2017 | Dynamic Programming | II | B.B |  |  |
|  | 21.03.2017 | Integer Linear Programming | II | B.B |  |  |
|  | 22.03.2017 | Local Search | II | B.B |  |  |
|  | 28.03.2017 | Simulated Annealing | II | B.B |  |  |
|  | 28.03.2017 | Tabu search, Genetic Algorithms | II | B.B |  |  |
|  |  | **Layout compaction, symbolic layout** | III |  |  |  |
|  | 29.03.2017 | Introduction | III | B.B |  |  |
|  | 01.04.2017 | Bellman-fold algorithm liao-wong algorithm | III | B.B |  |  |
|  | 01.04.2017 | Placement and partitioning | III | B.B |  |  |
|  | 04.04.2017 | Placement algorithm& partitioning the Kernighan-lin partitioning Algorithm | III | B.B |  |  |
|  | 06.04.2017 | Floorplanning concepts | III | B.B |  |  |
|  | 11.04.2017 | Routing, area routing algorithms | III | B.B |  |  |
|  | 12.04.2017 | Global routing algorithms | III | B.B |  |  |
|  | 25.04.2017 | Modelling and simulation, Gate Level Modeling | III | B.B |  |  |
|  | 26.04.2017 | Simulation, compiler driven and event driven simulation | III | B.B |  |  |
|  | 29.04.2017 | Switch level Modeling and simulation. | III | B.B |  |  |
|  |  | **LOGIC SYNTHESIS AND VERIFICATION** | IV |  |  |  |
|  | 29.04.2017 | Introduction | IV | B.B |  |  |
|  | 13.06.2017 | Basic issues and Terminology, | IV | B.B |  |  |
|  | 14.06.2017 | Binary-Decision diagram | IV | B.B |  |  |
|  | 17.06.2017 | ROBDD principles,construction, and variable ordering and Transition count testing, | IV | B.B |  |  |
|  | 17.06.2017 | Two – Level Logic Synthesis. | IV | B.B |  |  |
|  | 20.06.2017 | High Level Logic Synthesis. | IV | B.B |  |  |
|  | 21.06.2017 | Internal representation of the input algorithm | IV | B.B |  |  |
|  | 23.06.2017 | Allocation ,assignment and scheduling | IV | B.B |  |  |
|  | 23.06.2017 | Some Scheduling algorithms and High level Trannsformations. | IV | B.B |  |  |
|  |  | **PHYSICAL DESIGN AUTOMATION OF FPGA’S** | V |  |  |  |
|  | 24.06.2017 | FPGA Introduction | V | B.B |  |  |
|  | 28.06.2017 | FPGA technologies, | V | B.B |  |  |
|  | 30.06.2017 | Physical Design cycle for FPGA’s | V | B.B |  |  |
|  | 01.07.2017 | partitioning and routing for segmented models | V | B.B |  |  |
|  | 01.07.2017 | Routing algorithm | V | B.B |  |  |
|  | 05.07.2017 | partitioning and routing for staggered models. | V | B.B |  |  |
|  | 07.07.2017 | algorithm for segmented models and staggered models. | V | B.B |  |  |
|  |  | **PHYSICAL DESIGN AUTOMATION OF MCM’S:** | VI |  |  |  |
|  | 07.07.2017 | MCM technologies | VI |  |  |  |
|  | 08.07.2017 | MCM physical design cycle and partitioning. | VI | B.B |  |  |
|  | 08.07.2017 | Placement – Chip array based full custom approaches, | VI | B.B |  |  |
|  | 09.07.2017 | Routing – Maze routing, Multiple stage routing | VI | B.B |  |  |
|  | 11.07.2017 | Topologic routing, Integrated Pin – Distribution and Routing. | VI | B.B |  |  |
|  | 11.07.2017 | Routing of FMCM’s programmable MCM’s | VI | B.B |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**TEXT BOOKS:**

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, Johnwiley& Sons (Asia) Pvt. Ltd, 1999.

2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer

International Edition, 2005

**REFERENCE BOOKS:**

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993

2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

**FACULTY HEAD OF THE DEPARTMENT**