

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	14/2/14	Introduction of lowpower design an. over view	I	Black board		
2	14/2/14	Introduction to low-voltage lowpower design	II	I		
3	15/2/14	Limitations, Silicon-on-insulator	II	II		
4	20/2/14	MOS/Bic mos processes Introduction	II	II		
5	20/2/14	Bicmos processes	II	II		
6	24/2/14	Integration and isolation considerations	II	II		
7	27/2/14	Integrated considerations	II	II		
8	22/2/14	Analog/digital cmos process	II	II		
9	28/2/14	Introduction of low-voltage/lowpower cmos	II	II		
10	1/3/14	Bicmos processes.	II	II		
11	4/3/14	Deep submicron process,	II	II		
12	6/3/14	SoI cmos,	II	II		
13	7/3/14	lateral BJT on SoI.	II	II		
14	8/3/14	future trends/and directions of cmos/bicmos	II	I		
15	12/3/14	Introduction of device Behaviour and modelling	III	II		
16	14/3/14	Advanced mosfet models	II	I		
17	20/3/14	Limitation of mosfet models.	II	I		
18	21/3/14	Bipolar models	II	II		
19	27/3/14	Analytical and Experimental characterization	IV	II		
20	3/4/14	sub half micron mos devices.	II	II		

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21	3/4/14	MOSFET in a hybrid mode environment	IV	Blackboard		
22	4/4/14	Introduction of low-voltage low power logic circuits	IV			
23	4/4/14	Comparison of advanced BiCMOS digital circuits				
24	14/4/14	ESD-free BiCMOS process.				
25	19/4/14	Digital circuit operation				
26	19/4/14	Comparative evaluation				
27	24/5/14	CMOS and BiCMOS logic gates introduction	VI			
28	24/5/14	Conventional CMOS				
29	24/5/14	BiCMOS logic gates				
30	24/5/14	Performance evaluation				
31	29/5/14	Introduction of low power latches and flipflops				
32	29/5/14	Evolution of latches				
33	29/5/14	Flipflops - quality measure for latches				
34	5/6/14	and flipflops.				
35	5/6/14	Design perspective				
36	6/6/14	Review of low power latches.				
37	6/6/14	Review of flipflops				
38	7/6/14	Review of CMOS logic gates.				
39	12/6/14	Review of BiCMOS logic gates.				
40	13/6/14	Low power design overview				