**LESSON PLAN**

**Branch**: M.TECH **Semester**: I I **Subject** :DFTS

**Acadamic year:2016-17 faculty :A.JAYALAXMI**

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| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|  | 22.02.2017 | BASIC CONCEPTS: Reliability concepts | I | Black Board |  |  |
|  | 23.02.2017 | Failure & Faults | I | B.B |  |  |
|  | 24.02.2017 | Reliability and failure rate | I | B.B |  |  |
|  | 25.02.2017 | Relation between reliability and meantime between failure | I | B.B |  |  |
|  | 25.02.2017 | Maintainability and Availability | I | B.B |  |  |
|  | 01.03.2017 | Reliability of series, Parallel and Parallel-Series combinational circuits. | I | B.B |  |  |
|  | 03.03.2017 | FAULT TOLERANT DESIGN: Basic concepts | II | B.B |  |  |
|  | 04.03.2017 | Static, dynamic | II | B.B |  |  |
|  | 08.03.2017 | hybrid, Triple Modular Redundant System | II | B.B |  |  |
|  | 10.03.2017 | Self purging redundancy | II | B.B |  |  |
|  | 11.03.2017 | Siftout redundancy (SMR) | II | B.B |  |  |
|  | 15.03.2017 | SMR Configuration | II | B.B |  |  |
|  | 18.03.2017 | Use of error correcting code | II | B.B |  |  |
|  | 18.03.2017 | Use of error correcting code | II | B.B |  |  |
|  | 21.03.2017 | Time redundancy | II | B.B |  |  |
|  | 22.03.2017 | software redundancy | II | B.B |  |  |
|  | 28.03.2017 | SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits | III | B.B |  |  |
|  | 28.03.2017 | Basic concepts of Self checking circuits | III | B.B |  |  |
|  | 29.03.2017 | Design of Totally Self Checking checker | III | B.B |  |  |
|  | 01.04.2017 | Design of Totally Self Checking checker | III | B.B |  |  |
|  | 01.04.2017 | Checkers using m out of n codes | III | B.B |  |  |
|  | 04.04.2017 | Checkers using m out of n codes | III | B.B |  |  |
|  | 06.04.2017 | Berger code, | III | B.B |  |  |
|  | 11.04.2017 | Low cost residue code | III | B.B |  |  |
|  | 12.04.2017 | Low cost residue code | III | B.B |  |  |
|  | 25.04.2017 | FAIL SAFE DESIGN: Strongly fault secure circuits | IV | B.B |  |  |
|  | 26.04.2017 | Strongly fault secure circuits | IV | B.B |  |  |
|  | 29.04.2017 | fail-safe design of sequential circuits using partition theory and Berger code | IV | B.B |  |  |
|  | 29.04.2017 | fail-safe design of sequential circuits using partition theory and Berger code | IV | B.B |  |  |
|  | 13.06.2017 | fail-safe design of sequential circuits using partition theory and Berger code | IV | B.B |  |  |
|  | 14.06.2017 | totally self-checking PLA design | IV | B.B |  |  |
|  | 17.06.2017 | totally self-checking PLA design | IV | B.B |  |  |
|  | 17.06.2017 | DESIGN FOR TESTABILITY FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS: Basic concepts of testability | V | B.B |  |  |
|  | 20.06.2017 | controllability and observability | V | B.B |  |  |
|  | 21.06.2017 | the Reed Muller’s expansion technique | V | B.B |  |  |
|  | 23.06.2017 | the Reed Muller’s expansion technique | V | B.B |  |  |
|  | 23.06.2017 | OR-AND-OR design | V | B.B |  |  |
|  | 24.06.2017 | OR-AND-OR design | V | B.B |  |  |
|  | 28.06.2017 | use of control and syndrome testable design | V | B.B |  |  |
|  | 30.06.2017 | use of control and syndrome testable design | V | B.B |  |  |
|  | 01.07.2017 | Scan Registers | V | B.B |  |  |
|  | 01.07.2017 | Scan Registers | V | B.B |  |  |
|  | 05.07.2017 | Classic Scan Design | V | B.B |  |  |
|  | 07.07.2017 | Level Sensitive Scan Design (LSSD) | V | B.B |  |  |
|  | 07.07.2017 | Level Sensitive Scan Design (LSSD) | V | B.B |  |  |
|  | 08.07.2017 | Theory and operation of LFSR | VI | B.B |  |  |
|  | 08.07.2017 | LFSR as Signature analyzer | VI | B.B |  |  |
|  | 09.07.2017 | LFSR as Signature analyzer | VI | B.B |  |  |
|  | 11.07.2017 | Multiple-input Signature Register | VI | B.B |  |  |
|  | 11.07.2017 | BUILT IN SELF TEST: BIST concepts | VI | B.B |  |  |
|  | 12.07.2017 | Test pattern generation for BIST exhaustive testing | VI | B.B |  |  |
|  | 12.07.2017 | pseudorandom testing | VI | B.B |  |  |
|  | 14.07.2017 | pseudo exhaustive testing | VI | B.B |  |  |
|  | 15.07.2017 | constant weight patterns | VI |  |  |  |
|  | 15.07.2017 | Generic offline BIST architecture | VI | B.B |  |  |