**LESSON PLAN**

**Subject Code & Name: VLSID**

**Branch: E.C.E-A Class / Semester: III/II Academic Year:2015-16**

**Faculty: V.Laxmi**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **Introduction** | **I** |  |  |  |
| 1 | 04.01.16 | Introduction to IC technology |  | PPT |  |  |
| 2 | 04.01.16 | the IC era, MOS and related VLSI technology and basic MOS transistors. |  | PPT |  |  |
| 3-9 | 06.01.16 to 20.01.16 | IC production process |  | PPT |  |  |
| 10-12 | 21.01.16 to 25.01.16 | MOS and CMOS fabrication process |  | PPT |  |  |
| 13 | 27.01.16 | Bi-CMOS technology |  | PPT |  |  |
| 14 | 28.01.16 | comparison between CMOS and bipolar technologies |  | PPT |  |  |
|  |  | **Basic electrical properties of MOS and Bi-CMOS circuits** | **II** |  |  |  |
| 15 | 01.02.16 | Ids – Vds relationship |  | CB |  |  |
| 16 | 01.02.16 | , aspects of MOS transistor: threshold voltage, trans-conductance, output conductance and figure of merit. |  | CB |  |  |
| 17 | 03.02.16 | Pass transistor, MOS inverter, |  | CB |  |  |
| 18 | 04.02.16 | determination of pull-up to pull-down ratio of NMOS. |  | CB |  |  |
| 19 | 08.02.16 | NMOS inverter driven by another NMOS inverter and driven through one or more pass transistors |  | CB |  |  |
| 20 | 08.02.16 | . Alternative forms of pull-up, |  | CB |  |  |
| 21 | 15.02.16 | CMOS inverter, |  | CB |  |  |
| 22 | 15.02.16 | MOS transistor circuit model, |  | CB |  |  |
| 23 | 17.02.16 | Bi-CMOS inverter and latch-up in CMOS circuits. |  | CB |  |  |
|  |  | **VLSI Circuit design process** | **III** |  |  |  |
| 24 | 18.02.16 | VLSI design flow, |  | PPT |  |  |
| 25-26 | 22.02.16 | layers of abstraction and stick diagrams. |  | PPT |  |  |
| 27 | 24.02.16 | Design rules for wires, |  | PPT |  |  |
| 28 | 25.02.16 | contacts and transistor |  | PPT |  |  |
| 29-30 | 29.02.16 | layout diagrams for NMOS and CMOS inverters and gates. |  | PPT |  |  |
| 31 | 02.03.16 | Scaling models |  | CB |  |  |
| 32 | 03.03.16 | scaling factors for device parameters |  | CB |  |  |
| 33 | 07.03.16 | scaling factors for device parameters |  | CB |  |  |
| 34 | 07.03.16 | limitations of scaling. |  | CB |  |  |
|  |  | **Gate Level Design** | **IV** |  |  |  |
| 35 | 07.03.16 | Logic gates and other complex gates |  | CB |  |  |
| 36 | 09.03.16 | switch logic, |  | CB |  |  |
| 37-38 | 10.03.16&  14.03.16 | alternate gate circuits. |  | CB |  |  |
| 39 | 14.03.16 | Sheet resistance (Rs) and its concept to MOS |  | CB |  |  |
| 40 | 21.03.16 | . Area capacitance. |  | CB |  |  |
| 41 | 21.03.16 | calculations, |  | CB |  |  |
| 42 | 23.03.16 | delays, |  | CB |  |  |
| 43 | 24.03.16 | driving large capacitive load, |  | CB |  |  |
| 44 | 28.03.16 | wiring capacitances, |  | CB |  |  |
| 45 | 28.03.16 | fan-in and fan-outs and choice of layers |  | CB |  |  |
| 46 | 31.03.16 | Shifters, adders, |  | PPT |  |  |
| 47 | 04.04.16 | ALUs, |  | PPT |  |  |
| 48 | 04.04.16 | multipliers |  | PPT |  |  |
| 49 | 06.04.16 | parity generators |  | PPT |  |  |
|  |  | **Design Methods** | **V** |  |  |  |
| 50-51 | 07.04.16 & 11.04.16 | Design-capture tools |  | CB |  |  |
| 52 | 11.04.16 | design- verification tools |  | CB |  |  |
| 53 | 13.04.16 | Need for CMOS testing, |  | CB |  |  |
| 54 | 1404.16 | manufacturing test principles |  | CB |  |  |
| 55 | 16.04.16 | design strategies for test. |  | CB |  |  |
| 56 | 19.04.16 | . Chip level test techniques |  | CB |  |  |
| 57 | 25.04.16 | system level test techniques |  | CB |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION**