**LESSON PLAN**

**Branch**: III ECE ‘B’ **Semester**: II **Subject** : VLSI

**Acadamic year:2015-16 faculty :A.JAYALAXMI**

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| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|  |  | **Introduction** | I |  |  |  |
|  | 05.01.2016 | Introduction to IC Technology | I | Black Board |  |  |
|  | 05.01.2016 | The IC era, MOS and related VLSI technology and basic MOS transistors. | I | B.B |  |  |
| 3-9 | 08.01.2016 to  22.01.2016 | IC production process | I | B.B |  |  |
| 10-12 | 26.01.2016 to  28.01.2016 | MOS and CMOS fabrication process. | I | B.B |  |  |
| 13 | 29.01.2016 | Bi-CMOS technology | I | B.B |  |  |
| 14 | 29.01.2016 | Comparison between CMOS and bipolar technologies. | I | B.B |  |  |
|  |  | **Basic electrical properties of MOS and Bi-CMOS circuits** | II |  |  |  |
| 15 | 02.02.2016 | Ids – Vds relationship | II | B.B |  |  |
| 16 | 04.02.2016 | Aspects of MOS transistor: threshold voltage, trans-conductance, output conductance and figure of merit. | II | B.B |  |  |
| 17 | 05.02.2016 | Pass transistor, MOS inverter | II | B.B |  |  |
| 18 | 05.02.2016 | Determination of pull-up to pull-down ratio of NMOS. | II | B.B |  |  |
| 19 | 09.02.2016 | NMOS inverter driven by another NMOS inverter and driven through one or more pass transistors | II | B.B |  |  |
| 20 | 16.02.2016 | Alternative forms of pull-up | II | B.B |  |  |
| 21 | 18.02.2016 | CMOS inverter | II | B.B |  |  |
| 22 | 19.02.2016 | MOS transistor circuit model | II | B.B |  |  |
| 23 | 19.02.2016 | Bi-CMOS inverter and latch-up in CMOS circuits. | II | B.B |  |  |
|  |  | **VLSI Circuit design process & Scaling of MOS circuits** | III |  |  |  |
| 24 | 23.02.2016 | VLSI design flow, | III | B.B |  |  |
| 25,26 | 25.02.2016 | layers of abstraction | III |  |  |  |
| 27 | 26.02.2016 | stick diagrams | III | B.B |  |  |
| 28 | 26.02.2016 | Design rules for wires | III | B.B |  |  |
| 29 | 01.02.2016 | contacts and transistor | III | B.B |  |  |
| 30 | 03.02.2016 | layout diagrams for NMOS & CMOS inverters and gates. | III | B.B |  |  |
| 31 | 03.02.2016 | Scaling models, | III | B.B |  |  |
| 32 | 04.02.2016 | Scaling factors | III | B.B |  |  |
| 33 | 04.02.2016 | Device parameters | III | B.B |  |  |
| 34 | 08.02.2016 | Limitations of scaling. | III | B.B |  |  |
|  |  | **Gate Level Design& Basic circuit concepts** | IV |  |  |  |
| 35 | 10.03.2016 | Logic gates and other complex gates | IV |  |  |  |
| 36 | 11.03.2016 | Switch logic | IV | B.B |  |  |
| 37,38 | 11.03.2016 | Alternate gate circuits. | IV | B.B |  |  |
| 39 | 15.03.2016 | Sheet resistance (Rs) and its concept to MOS. | IV | B.B |  |  |
| 40 | 22.03.2016 | Area capacitance | IV | B.B |  |  |
| 41 | 24.03.2016 | calculations | IV | B.B |  |  |
| 42 | 24.03.2016 | delays | IV | B.B |  |  |
| 43 | 25.03.2016 | driving large capacitive load | IV | B.B |  |  |
| 44 | 25.03.2016 | wiring capacitances | IV | B.B |  |  |
| 45 | 29.03.2016 | fan-in and fan-outs and choice of layers. | IV | B.B |  |  |
| 46 | 01.04.2016 | Subsystem Design, Shifters adders, | IV | B.B |  |  |
| 47 | 01.04.2016 | ALUs | IV | B.B |  |  |
| 48 | 05.04.2016 | multipliers | IV | B.B |  |  |
| 49 | 07.04.2016 | Parity generators. | IV | B.B |  |  |
|  |  | **Design Methods & CMOS Testing** | V |  |  |  |
| 50 | 08.04.2016 | Design-capture tools | V | B.B |  |  |
| 51 | 08.04.2016 | Design- verification tools. | V | B.B |  |  |
| 52 | 12.04.2016 | Need for CMOS testing | V | B.B |  |  |
| 53 | 13.04.2016 | Manufacturing test principles | V | B.B |  |  |
| 54 | 15.04.2016 | Design strategies for test. | V | B.B |  |  |
| 55 | 19.04.2016 | Chip level test techniques | V | B.B |  |  |
| 56 | 21.04.2016 | System level test techniques. | V | B.B |  |  |
| 57 | 22.04.2016 | Revision | V | B.B |  |  |

**Text books:**

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005.
2. Principles of CMOS VLSI Design – Weste and Eshraghian, Pearson Education, 1999.

**Reference books:**

1. VLSI Design – Debaprasad Das, Oxford university press, 2010.
2. VLSI Design – A.Albert Raj and T.Latha, PHI Learing private limited 2010.
3. ASIC design - Smith.