# LESSON PLAN

**Branch**: I M.Tech **Semester**: II **Subject** : AVDA

# Acadamic year: 2014-15 faculty :Swathi jallu

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| Period | Date (Tentative) | Topic | Unit No. | Teaching  Methodolo gy | Remar ks | Corrective Action upon Review |
|  |  | **PRELIMINARIES** | I |  |  |  |
| 1. | 22.02.2016 | Introduction to Design Methodologies The VLSI Design  problem Gaskis Y-Chart | I | Black Board |  |  |
| 2. | 23.02.2016 | The VLSI Design problem  Gaskis Y-Chart | I | B.B |  |  |
| 3. | 24.02.2016 | Design Actions ,Design methods and Technologies. | I | B.B |  |  |
| 4. | 25.02.2016 | VLSI Design Automation tools | I | B.B |  |  |
| 5. | 25.02.2016 | Tr-level design layout design,  verification. | I | B.B |  |  |
| 6. | 01.03.2016 | Algorithm Graph Theroy and  Terminology | I | B.B |  |  |
| 7. | 03.03.2016 | Dta Structures for the representation of graphs,  Computational Complexity | I | B.B |  |  |
| 8. | 04.03.2016 | Graph algorithms-DFS,BFS |  |  |  |  |
| 9. | 08.03.2016 | Dijkstra’s shortest path algorithm,  prims algorithm | I | B.B |  |  |
| 10. | 10.03.2016 | Tractable and Intractable  Problems | I | B.B |  |  |
|  | 11.03.2016 | **GENERAL PURPOSE METHO**  **FORCOMBINATIONAL OPTIMIZATION** | **D** II |  |  |  |
| 11. | 15.03.2016 | Introduction |  | B.B |  |  |
| 12. | 18.03.2016 | Travelling salesman problem Backtracking | II | B.B |  |  |
| 13. | 18.03.2016 | Branch and Bound, | II | B.B |  |  |
| 14. | 21.03.2016 | Dynamic Programming | II | B.B |  |  |
| 15. | 22.03.2016 | Integer Linear Programming | II | B.B |  |  |
| 16. | 28.03.2016 | Local Search | II | B.B |  |  |
| 17. | 28.03.2016 | Simulated Annealing | II | B.B |  |  |
| 18. | 29.03.2016 | Tabu search, Genetic Algorithms | II | B.B |  |  |

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|  |  | **Layout compaction, symbol**  **layout** | III |  |  |  |
| 19. | 01.04.2016 | Introduction | III | B.B |  |  |
| 20. | 04.04.2016 | Bellman-fold algorithm liao-  wong algorithm | III | B.B |  |  |
| 21. | 06.04.2016 | Placement and partitioning | III | B.B |  |  |
| 22. | 11.04.2016 | Placement algorithm& partitioning the Kernighan-lin  partitioning Algorithm | III | B.B |  |  |
| 23. | 12.04.2016 | Floorplanning concepts | III | B.B |  |  |
| 24. | 25.04.2016 | Routing, area routing algorithms | III | B.B |  |  |
| 25. | 26.04.2016 | Global routing algorithms | III | B.B |  |  |
| 26. | 29.04.2016 | Modelling and simulation, Gate Level Modeling | III | B.B |  |  |
| 27. | 29.04.2016 | Simulation, compiler driven and event driven simulation | III | B.B |  |  |
| 28. | 13.06.2016 | Switch level Modeling and  simulation. | III | B.B |  |  |
|  |  | **LOGIC SYNTHESIS AND**  **VERIFICATION** | IV |  |  |  |
| 29. | 14.06.2016 | Introduction | IV | B.B |  |  |
| 30. | 17.06.2016 | Basic issues and Terminology, | IV | B.B |  |  |
| 31. | 17.06.2016 | Binary-Decision diagram | IV | B.B |  |  |
| 32. | 20.06.2016 | ROBDD principles,construction, and variable ordering and  Transition count testing, | IV | B.B |  |  |
| 33. | 21.06.2016 | Two – Level Logic Synthesis. | IV | B.B |  |  |
| 34. | 23.06.2016 | High Level Logic Synthesis. | IV | B.B |  |  |
| 35. | 23.06.2016 | Internal representation of the input  algorithm | IV | B.B |  |  |
| 36. | 24.06.2016 | Allocation ,assignment and  scheduling | IV | B.B |  |  |
| 37. | 28.06.2016 | Some Scheduling algorithms and  High level Trannsformations. | IV | B.B |  |  |
|  |  | **PHYSICAL DESIGN**  **AUTOMATION OF FPGA’S** | V |  |  |  |
| 38. | 30.06.2016 | FPGA Introduction | V | B.B |  |  |
| 39. | 01.07.2016 | FPGA technologies, | V | B.B |  |  |
| 40. | 01.07.2016 | Physical Design cycle for FPGA’s | V | B.B |  |  |
| 41. | 05.07.2016 | partitioning and routing for | V | B.B |  |  |
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|  |  | segmented models |  |  |  |  |
| 42. | 07.07.2016 | Routing algorithm | V | B.B |  |  |
| 43. | 08.07.2016 | partitioning and routing for  staggered models. | V | B.B |  |  |
| 44. | 09.07.2016 | algorithm for segmented models  and staggered models. | V | B.B |  |  |
|  |  | **PHYSICAL DESIGN**  **AUTOMATION OF MCM’S:** | VI |  |  |  |
| 45 | 11.07.2016 | MCM technologies | VI |  |  |  |
| 46 | 12.07.2016 | MCM physical design cycle and  partitioning. | VI | B.B |  |  |
| 47 | 12.07.2016 | Placement – Chip array based full  custom approaches, | VI | B.B |  |  |
| 48 | 14.07.2016 | Routing – Maze routing, Multiple  stage routing | VI | B.B |  |  |
| 49 | 15.07.2016 | Topologic routing, Integrated Pin  – Distribution and Routing. | VI | B.B |  |  |
| 50 | 15.07.2016 | Routing of FMCM’s  programmable MCM’s | VI | B.B |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**TEXT BOOKS:**

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, Johnwiley& Sons (Asia) Pvt. Ltd, 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer International Edition, 2005

# REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

# FACULTY HEAD OF THE DEPARTMENT